

ABSTRACT OF THE DISCLOSURE

A parallel data outputting circuit equipped with a data inversion function, comprises P number of data comparator means, P number of majority
5 decision circuits, P number of inversion flag generating means and P number of data inversion circuits, these being activated in parallel in one cycle. In generating an inversion flag indicating whether or not the parallel data are to be inverted and output in the inverted state, inversion flags are calculated from outputs of the inversion flag generating means
10 and the inversion flag generating means of a cycle directly previous to a current cycle.